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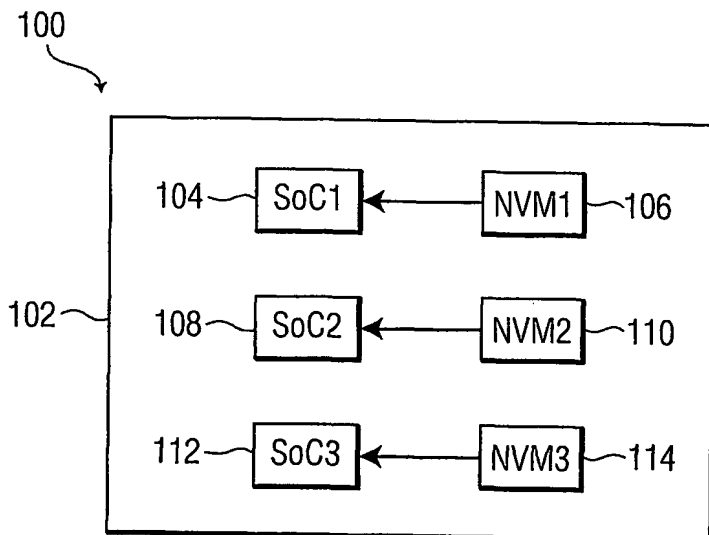
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(54) Title: CODE DOWNLOAD IN A SYSTEM HAVING MULTIPLE INTEGRATED CIRCUITS WITH JTAG CAPABILITY



(57) Abstract: An electronic product (500) including a first integrated circuit (502) coupled to a first memory (506) and at least a second integrated circuit (508, 512) coupled (516, 518, 520) to the first integrated circuit. The first integrated circuit loads information, such as a first code image, from the first memory into the first integrated circuit, and executes at least a portion of the first code image. In response to such code execution, the first integrated circuit reads information, such as a second code image, from the first memory and transmits that information to the second integrated circuit. The interface between the first and second integrated circuits for transmission of the information may be a test circuitry (522, 528, 526, 524) interface such as JTAG circuitry. In one embodiment

program code is transferred from a single external memory through a first integrated circuit to one or more downstream integrated circuits by way of serially connected JTAG data and control pins.



EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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